

Fayetteville State University
College of Basic and Applied Sciences
Department of Mathematics and Computer Science
CSC 303 – 01, Computer Organization and Architecture II
Spring 2010

I. Locator Information:

Instructor: Sambit Bhattacharya

Course # and Name: CSC303 – 01,

Computer Organization and Architecture II

Semester Credit Hours: 3.00

Day, Time and Location Class Meets: 10:00-10:50 am, MWF, Butler 317 TR: 10:45 – 11:45 am & 2 – 3:30 pm

Total Contact Hours for Class: 46

Email address: sbhatac@uncfsu.edu

Office Location: SBE 310

Office hours: MWF 2:50 – 3:50 pm &

Other hours by appointment only

Office Phone: 910 672 1156

FSU Policy on Electronic Mail: Fayetteville State University provides to each student, free of charge, an electronic mail account (username@uncfsu.edu) that is easily accessible via the Internet. The university has established FSU email as the primary mode of correspondence between university officials and enrolled students. Inquiries and requests from students pertaining to academic records, grades, bills, financial aid, and other matters of a confidential nature must be submitted via FSU email. Inquiries or requests from personal email accounts are not assured a response. The university maintains open-use computer laboratories throughout the campus that can be used to access electronic mail.

Rules and regulations governing the use of FSU email may be found at
<http://www.uncfsu.edu/PDFs/EmailPolicyFinal.pdf>

II. Course Description: This course is a continuation of CSC 201 which covers many aspects of computer architecture and implementation. Topics covered include pipelining, instruction-level parallelism; advanced cache and memory-hierarchy design issues; design issues for shared memory multiprocessors; storage systems and design of input/output systems; architectural implications for networks and distributed systems. In this course a rigorous quantitative approach is taken to examine different system design tradeoffs.

Prerequisite: CSC201.

III. Disabled Student Services: In accordance with Section 504 of the 1973 Rehabilitation Act and the Americans with Disabilities Act (ACA) of 1990, if you have a disability or think you have a disability to please contact the Center for Personal Development in the Spaulding Building, Room 155 (1st Floor); 910-672-1203.

IV. Textbook:

1. *Required Textbook:* Patterson, David A. and John L. Hennessey, *Computer Organization and Design: The Hardware/Software Interface, Third Edition*, Morgan Kaufmann, 2004, ISBN-10: 1558606041, ISBN-13: 978-1558606043.
2. *Required Textbook:* Britton, Robert, *MIPS Assembly Language Programming, First Edition*, Prentice Hall, 2003, ISBN-10: 0131420445, ISBN-13: 978-0131420441.
3. *Optional Textbook (purchase not required):* Lala, Parag K., *Principles of Modern Digital Design*, Wiley-Interscience, 2007, ISBN-10: 0470072962, ISBN-13: 978-0470072967.
4. *Optional Textbook (purchase not required):* Sweetman, Dominic, *See MIPS Run, Second Edition*, Morgan Kaufmann, 2006, ISBN-10: 0120884216, ISBN-13: 978-0120884216.
5. *Optional Textbook (purchase not required):* Vahid, Frank, *Digital Design*, John Wiley & Sons, 2006, ISBN-10: 0470044373, ISBN-13: 978-0470044377.

V. Student Learning Outcomes:

Upon completion of this course, students will be able to:

1. Design combinational logic circuits, sequential logic circuits, datapath components such as registers, adders etc.
2. Design a simple datapath and a pipelined datapath for a processor that can execute instruction sets like MIPS.
3. Simplify and solve Boolean equations, translate between the following representations: Boolean equations, truth table, and logic gates.
4. Measure, report and summarize the performance of a computer.
5. Measure cache performance.

6. Measure the performance of I/O such as the disk and file system.
7. Describe the major hardware factors that are keys to the effectiveness of an entire system of hardware and software.
8. Describe the principles of cache design; identify ways of improving cache performance.
9. Describe virtual memory organization.
10. Describe the principles and techniques used in implementing a processor.
11. Describe how processors, memory and I/O devices are connected.

VI. Course Requirements and Evaluation Criteria:

a. Grading Scale –

Grade	Total point range	Credit Hours	Quality Points	Meaning
A	90% – 100%	Hours attempted and earned	4 per credit hour;	Exceptionally high
B	80% – 89%	Hours attempted and earned	3 per credit hour	Good
C	65% – 79%	Hours attempted and earned	2 per credit hour	Satisfactory
D	55% – 64%	Hours attempted and earned	1 per credit hour	Marginally passing
F	below 55%	Hours attempted – Not earned	0 per credit hour	Failing
FN		Hours attempted – Not earned	0 per credit hour	Failing due to non-attendance. (Student registered, but <u>never</u> attended.)
W		Hours attempted – Not earned	No impact on GPA	Class withdrawal prior to deadline (see Academic Calendar)
P		Hours attempted and earned	No impact on GPA	Satisfactory - Assigned only in classes specified as Pass/Fail
WU		Hours attempted – Not earned	No impact on GPA	Withdrawal from all classes for semester or term
AU		Hours attempted – Not earned	No impact on GPA	Auditing

- b. Attendance Requirements –The attendance requirements for regular courses are as follows: students are expected to attend all class meetings, laboratories, and other instructional sessions for this course. Students are also expected to arrive to class on time and remain in class for the entire scheduled period. When students must miss class(es) for unavoidable reasons, i.e., illness, family emergencies, or participation in official university sponsored activities – they are responsible for informing faculty of the reasons for the absences, in advance if possible. Missed assignments, labs, quizzes and exams can only be made up for by explicit permission from the instructor. In order to receive this permission the student has to provide convincing evidence (e.g. doctor’s note) that the absence was due to an unavoidable reason. During the first half of the semester/term, faculty will assign an interim grade of “EA,” Excessive Absences, for students whose class absences exceed 10% of the total contact hours for the class. Students who receive EA interim grades must either withdraw from the class or resume attendance. Students who resume attendance must consult with the instructor about completion of missed assignments. The EA is not a final grade, so students who are assigned an interim grade of EA, but do not withdraw from the class, will receive a final grade based on the evaluation criteria for the class. **Please note that the WN grade is no longer in effect. Students must not expect faculty to withdraw them from classes. For more information about this and the new ‘X’ grade please read the attached document (last page of syllabus) titled “Revision of grades – student responsibilities”.**
- c. Graded Assignments and Value of Each Assignment –
 - i. Two tests (best one taken out of two) for a total of 20%
 - ii. Final test worth 30%
 - iii. Eight problem solving assignments/projects worth a total of 40%
 - iv. Class participation and attendance worth 10%

- v. **Note:** By new FSU policy interim grades of X and EA will be assigned by the instructor based on class attendance (for more read “Revision of Grades – Student Responsibilities” on the last page). Since this is a purely online course attendance will be measured by the instructor as the student’s degree of class participation through discussion boards as well as timeliness of assignment, quiz and test submissions. Students will receive X or EA within the specified time limits if he or she posts no messages on the discussion boards and/or receives zero grades on assignments, quizzes and tests.
- d. Assignments are posted in Blackboard under “Assignments” and must be submitted on or before the due date. Unless explicitly stated,
 - i. All assignments must be submitted online via the View/Complete link found in each assignment.
 - ii. Assignments submitted online via the View/Complete link must be turned in as a file attachment.
 - iii. Do not email assignments to your instructor.
 - iv. Do not submit assignments to the Digital Drop Box.
 - v. Assignments submitted via email to the instructor or the digital drop box will not be accepted.
- e. Policy on Missed or Late Assignments - tests, quizzes, assignments and projects missed due to an unavoidable reason can be made up only with the instructor’s permission. In order to receive this permission the student has to provide convincing evidence (e.g. doctor’s note) that the absence was due to an unavoidable reason. There is a penalty of 5% for each day a project or assignment is overdue. Project or assignment submissions that are more than a week overdue will not be accepted for grading.
- f. Communication policy: Every student must have an active and working email address. Every student must post his/her email address in Blackboard and make the email address visible using the Personal Information Tools.
 - i. To edit your personal information in Blackboard, follow these steps:
 1. Click on Tools
 2. Click Personal Information
 3. Click Edit Personal Information
 4. Enter your correct and active email address in the appropriate box
 5. Click Submit
 6. Click OK
 7. Click Privacy Options
 8. Check the first box which indicates Email Address
 9. Click Submit
 10. Click OK
 - ii. FSU Policy on Electronic Mail: *Refer to the box in the first page of this syllabus.*
 - iii. Email sent to the instructor must comply with the following procedure:
 1. Course name CSC303 must be written in the subject box:
 2. Include your first and last names after your email message
 3. Email that does not follow the communication policy and procedure will not receive a response.
 4. Email without the course name CSC303 in the subject box will not be opened.
 5. Email without a first and last name will not receive a response
- g. Student responsibilities:
 1. Student should check their email and Blackboard daily for announcements regarding this course.
 2. Students must have their own computer which runs on the Windows operating systems. Optionally students may also have a Linux operating system installed on the same (dual boot) or different machine. Students are discouraged from using the computer at work or library since several types of software programs will be used for instruction in this course and students will have to install those programs on their own machines to be able to run them.
 3. There are a total of 2 tests (best 1 taken from 2) and a cumulative final exam. Make up tests will only be available to students with documented, excused absences.
 4. Each student must independently complete all tests, homeworks and programming projects unless otherwise specified. However, you may discuss the assignments (in general) with each other.
 5. Class participation is an essential part of your final grade.
 6. Five percent (5%) of the total points will be deducted from each school day a programming assignment is overdue.

Please note: If these evaluation criteria must be revised because of extraordinary circumstances, the instructor will distribute an amendment to the syllabus.

Student Behavior Expectations: - The instructor will respect all students and will make every effort to maintain a classroom climate that promotes learning for all students. Students must accept their responsibility for maintaining a positive classroom environment by abiding by the following rules:

1. Students are expected to arrive to class on time, remain in class until dismissed by the instructor, and refrain from preparing to leave class until it is dismissed.
2. Student/teacher relationships, as well as relationships among peers, must be respectful at all times.
3. Students are not permitted to wear headphones or other paraphernalia that may be distracting to the classroom environment.
4. Students must refrain from any activity that will disrupt the class; this includes turning off cell phones and pagers.
5. Students are not permitted to use profanity in the classroom.
6. Students will not pass notes or carry on private conversations while class is being conducted.

Consequences for Failing to Meet Behavioral Expectations: The first time a student violates one of these rules, the instructor will warn him or her privately, either after class or before the next class. (Faculty members reserve the right to warn students publicly if needed.) The second time a student violates the guidelines, the instructor may deduct as many as twenty points from the student's next exam grade. If a student violates the guidelines three times, the instructor will report the student to the Dean of Students for disciplinary action according to the FSU Code of Student Conduct.

VII. Academic Support Resources – Apart from FSU Blackboard this course will use the list of resource websites provided under External Links of Blackboard. Students should regularly access FSU Blackboard and the resources websites to stay current in this course. For complete information look under “Academic Support” in Blackboard.

VIII. Academic Integrity Policy - Because plagiarism is so serious and is becoming increasingly prevalent in higher education, Fayetteville State University has adopted the following procedures for dealing with this form of academic dishonesty. Any student found guilty of academic dishonesty will be subject to disciplinary actions as described in the student handbook. Academic dishonesty includes, but is not limited to the following: cheating, plagiarism, complicity in academic dishonesty (helping or attempting to help another student cheat) and misrepresentation to avoid academic work (e.g. fabricating excuses of illness, injury, accident, family death, etc. to avoid the timely submission of academic work or test taking).

IX. Disability Policy - The university provides for the matriculation of all students without regard to sex, race, religion, or disability. The university continues to be sensitive to the identification of possible barriers to students with disabilities and attempts to make reasonable accommodations for these students. Students with disabilities who need assistance in utilizing university services should register with the Center for Personal Development as soon as they are admitted to the university. (<http://www.uncfsu.edu/fsuretention/Student%20Affairs.pdf>). Also refer to item III on the first page of the syllabus for Disabled Student Services

X. Course Outline and Assignment Schedule:

WEEK	LECTURE TOPICS & ACTIVITIES
FIRST DATES: 01/11 – 01/15	SYLLABUS AND POLICIES FOR THE COURSE INTRODUCTIONS
SECOND DATES: 01/18 – 01/22	TEXTBOOK APPENDIX B
THIRD DATES: 01/25 – 01/29	TEXTBOOK APPENDIX C

FOURTH DATES: 02/01 – 02/05	TEXTBOOK CHAPTER 5
FIFTH DATES: 02/08 – 02/12	TEXTBOOK CHAPTER 5 CONTINUED
SIXTH DATES: 02/15 – 02/19	TEXTBOOK CHAPTER 6
SEVENTH DATES: 02/22 – 02/26	TEXTBOOK CHAPTER 6 CONTINUED
EIGHTTH DATES: 03/01 – 03/05	TEST 1
NINTH DATES: 03/08 – 03/12	BREAK
TENTH DATES: 03/15 – 03/19	TEXTBOOK CHAPTER 7
ELEVENTH DATES: 03/22 – 03/26	TEXTBOOK CHAPTER 7 CONTINUED
TWELFTH DATES: 03/29 – 04/02	TEXTBOOK CHAPTER 8
THIRTEENTH DATES: 04/05 – 04/09	TEXTBOOK CHAPTER 8 CONTINUED
FOURTEENTH DATES: 04/12 – 04/16	TEST 2
FIFTEENTH DATES: 04/19 – 04/23	TEXTBOOK CHAPTER 9
SIXTEENTH DATES: 04/26 – 04/30	REVIEW
FINAL EXAMS FOR GRADUATING SENIORS 04/25 TO 04/29 FINAL EXAMS FOR STUDENTS NOT GRADUATING 04/30 TO 05/06	

XI. Teaching Strategies: The primary teaching strategies for this course will be lectures and discussion. You are strongly encouraged to participate in any discussion being held in the discussion boards. Programs in assembly and some high level languages will be used to demonstrate how programs interact with the underlying hardware. In addition to solving tests, quizzes and problem solving assignments students will complete short programming projects in this course.

XII. Bibliography:

1. Hennessy, J. L., and D. A. Patterson [2003]. *Computer Architecture: A Quantitative Approach*, third edition, Morgan Kaufmann Publishers, San Francisco.

2. Bayko, J. [1996]. "Great Microprocessors of the Past and Present," available at www.mkp.com/books_catalog/cod/links.htm.
3. Kane, G., and J. Heinrich [1992]. *MIPS RISC Architecture*, Prentice Hall, Englewood Cliffs, NJ.
4. Koren, I. [2002]. *Computer Arithmetic Algorithms*, second edition, A. K. Peters, Natick, MA.
5. Levy, H. M., and R. H. Eckhouse, Jr. [1989]. *Computer Programming and Architecture: The VAX*, Second ed., Digital Press, Bedford, MA.
6. Bhandarkar, D., and D. W. Clark [1991]. "Performance from architecture: Comparing a RISC and a CISC with similar hardware organizations," *Proc. Fourth Conf. on Architectural Support for Programming Languages and Operating Systems*, IEEE/ACM (April), Palo Alto, CA, 310–19.
7. Kogge, P. M. [1981]. *The Architecture of Pipelined Computers*, New York: McGraw-Hill.
8. LaMarca, A. and R. E. Ladner [1996]. "The influence of caches on the performance of heaps," *ACM J. of Experimental Algorithmics*, vol.1, www.jea.acm.org/1996/LaMarcaInfluence/.
9. Przybylski, S. A. [1990]. *Cache and Memory Hierarchy Design: A Performance-Directed Approach*, Morgan Kaufmann Publishers, San Francisco.
10. Silberschatz, A., P. Galvin, and G. Grange [2003]. *Operating System Concepts*, sixth edition, Addison-Wesley, Reading, MA.
11. Tanenbaum, A. [2001]. *Modern Operating Systems*, second edition, Prentice Hall, Upper Saddle River, NJ.
12. Brenner, P. [1997]. *A Technical Tutorial on the IEEE 802.11 Protocol* found on many Web sites.
13. Chen, P. M., E. K. Lee, G. A. Gibson, R. H. Katz, and D. A. Patterson [1994]. "RAID: High-performance, reliable secondary storage," *ACM Computing Surveys* 26:2 (June), 145–88.
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15. Amdahl, G. M. [1967]. "Validity of the single processor approach to achieving large scale computing capabilities," *Proc. AFIPS Spring Joint Computer Conf.*, Atlantic City, NJ, (April) 483–85.
16. Culler, D. E., and J. P. Singh, with A. Gupta [1998]. *Parallel Computer Architecture*, Morgan Kaufmann, San Francisco.
17. Hwang, K. [1993]. *Advanced Computer Architecture with Parallel Programming*, McGraw-Hill, New York.
18. Kozyrakis, C., and D. Patterson [2003]. "Scalable vector processors for embedded systems," *IEEE Micro* 23:6 (November–December), 36–45.
19. Pfister, G. F. [1998]. *In Search of Clusters: The Coming Battle in Lowly Parallel Computing*, second edition, Prentice-Hall, Upper Saddle River, NJ.
20. Sweetman, D. [1999]. *See MIPS Run*, Morgan Kaufmann Publishers, San Francisco, CA.
21. MIPS32™ Architecture for Programmers Volume I: Introduction to the MIPS32™ Architecture (<http://mips.com/content/Documentation/MIPSDocumentation/ProcessorArchitecture/ArchitectureProgrammingPublicationsforMIPS32/MD00082-2B-MIPS32INT-AFP-02.00.pdf/getDownload>)
22. MIPS32™ Architecture for Programmers Volume II: The MIPS32™ Instruction Set (<http://mips.com/content/Documentation/MIPSDocumentation/ProcessorArchitecture/ArchitectureProgrammingPublicationsforMIPS32/MD00086-2B-MIPS32BIS-AFP-02.00.pdf/getDownload>)
23. MIPS32™ Architecture for Programmers Volume III: The MIPS32™ Privileged Resource Architecture (<http://mips.com/content/Documentation/MIPSDocumentation/ProcessorArchitecture/ArchitectureProgrammingPublicationsforMIPS32/MD00088-2B-MIPS32PRV-AFP-02.00.pdf/getDownload>)

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25. Ciletti, M. D. [2002] *Advanced Digital Design with the Verilog HDL*, Englewood Cliffs, NJ: Prentice-Hall.
26. Katz, R. H. [2004]. *Modern Logic Design*, second edition, Reading, MA: Addison Wesley.